value which is generated from the counter by a timing signal which is generated from an MMV **522***d* and is synchronized with the timing of the timing signal SPP which is supplied from the pre-pit signal reproducing circuit.

The reason why the phase comparison can be accurately performed by the phase comparing circuit **522** even in a case where parts of sync signal as comparison target are formed at intervals different from the intervals of the other sync signal parts like pre-pit signals which are formed in the DVD-R 1 is as described in the phase comparing circuits **14** and **15**.

Namely, on the basis of the clock signal SCKV1 from the VCO, the signal in which the ramp signal having the sync frame period (1488 T) as a unit period in the recording format of the DVD-R 1 is sampled and held at the detection timing of the pre-information recorded on the information recording medium is used as a phase difference signal and the oscillating period of the clock signal SCKV1 which is generated from the VCO **521** is controlled. Even when the period at which the pre-pit signal comprising the sync pre-signal and the data pre-signal is detected changes on a sync frame unit basis, therefore, the clock signal SCKV1 in which the phase synchronizing state for a predetermined frequency is maintained can be formed.

According to the first aspect of the invention as described above, the phase difference, relative to the unit period as a period which is a fraction, by the division by an integer number, of the period of the pre-pits, is compared at timings when the pre-pit is detected and the rotation of the motor is controlled so as to set off the phase difference. Consequently, even when no pre-pit is derived at predetermined periodic intervals, a predetermined rotating state can be accurately obtained.

Therefore, even in an information recording medium, therefore, on which parts of the sync signals are at a recording interval that is deviated from predetermined intervals, information can be accurately recorded and reproduced by maintaining the accurate rotating state.

According to the second aspect of the invention, in addition to the effect of the first aspect of the invention, the unit period signal generator generates the monotonous increase signal having the unit period while the phase difference detector detects the phase difference on the basis of the amplitude value of the monotonous increase signal at the detection timing of the pre-pit, so that the phase difference can be detected by a simple process.

According to the third aspect of the invention, the coarse phase difference signal is obtained by comparing the phase difference relative to the unit period as a period which is a fraction, by the division by an integer number, of the period of intervals of the sync pits at the detection timings of the sync pits which are detected at relatively coarse intervals, the fine phase difference signal is obtained by comparing the phase difference for the unit period as a period which is a fraction, by the division by an integer number, of the period of intervals of the pre-pits at detection timings of the pre-pits that comprise the sync pre-signal and the data pre-signal and are detected at relatively dense intervals, and the addition phase difference signal is produced by adding the coarse phase difference signal and the fine phase difference signal. The rotation of the motor is controlled on the basis of the addition phase different signal so as to set off the phase difference. Even when no pre-pit is derived at predetermined periodic intervals, therefore, a predetermined rotating state can be accurately obtained. In addition, a rotation control of a higher precision can be carried out as compared with the rotation control by only the sync pits.

Even in an information recording medium in which parts of the sync signal are recorded at a recording interval that is deviated from predetermined intervals, therefore, the information can be accurately recorded and reproduced by maintaining an accurate rotating state.

The invention has been described above with reference to the preferred embodiments. The person with ordinary skill in the art should understand that various modifications and variations of the invention can be presumed. All of the modifications and variations are also incorporated in the scope of claim for a patent of the invention.

What is claimed is:

1. An information data recording apparatus for recording information data on an information recording medium having pre-pits which are formed at periodic intervals having a period that is m, m being an integer, times as large as a unit period in accordance with pre-information recorded at an interval which deviates from said periodic intervals by an interval that is k, k being an integer, where k<m, times said unit period in accordance with recording positions, said apparatus comprising:

a unit period signal generator which generates a periodic signal of said unit period;

a memory for temporarily storing said information data in synchronism with said periodic signal from said unit period signal generator and supplying said information data in synchronism with a clock signal;

a pre-pit signal reproducing circuit for detecting said pre-pits from said recording medium and generating a pre-pit signal;

a phase-locked loop circuit for generating said clock signal which is phase-locked with a jitter component contained in said pre-pit signal; and

a recording means for recording said information data supplied from said memory on said recording medium.

2. An information data recording apparatus as claimed in claim **1**, wherein said phase-locked loop circuit comprises:

a voltage controlled oscillator for generating said clock signal in accordance with a control voltage;

a phase comparator circuit for comparing said pre-pit signal generated by said pre-pit signal reproducing circuit with said clock signal generated by said voltage controlled oscillator and producing a phase comparison output signal; and

an amplitude and phase equalizing circuit for adjusting amplitude and phase of said phase comparison output signal of said phase comparator to produce said control voltage supplied to said voltage controlled oscillator.

3. An information data recording apparatus as claimed in claim **1**, further comprising a feed-forward circuit for eliminating a phase error in said information data supplied from said memory, said phase error corresponding to a residual phase error component of said clock signal generated by said phase-locked loop circuit.

4. An information data recording apparatus as claimed in claim **3**, wherein said feed-forward circuit comprises:

a second memory for storing said information data supplied from said memory in synchronism with said clock signal and supplying said information data to said recording means in synchronism with a second clock signal; and

a voltage controlled oscillator for generating said second clock signal in accordance with said phase comparison output signal of said phase comparator circuit.

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